Remarks

Claims 1, 3 - 7 and 12 - 17 are in the application. Reconsideration of the application is requested in light of the remarks following.

Applicant thanks the Examiner for indicating allowable subject matter in the application. Applicant's invention is directed to encapsulation of flip chip interconnects. The claimed methods for encapsulating flip chip interconnects include applying a limited quantity of encapsulating resin to the interconnect side of an integrated circuit chip.

A wide variety of materials are useful as encapsulating resins (sometimes known as "potting resins"), and the various materials differ in some physical characteristics; for example, encapsulating resins are available in a wide range of viscosities, thermal conductivities, thermal expansion coefficients, adhesion, color, hardness, *etc*. However, as is well known in the art, **encapsulating resins necessarily** have in common the characteristic that they **are electrical insulators**; that is, encapsulating resins are substantially electrically nonconductive, having high dielectric constants and, in many applications, high dielectric strength.

The points raised in the Office action will now be addressed.

Rejections under 35 U.S.C. § 102(b)

Claims 1, 4 - 7, 12 and 14 - 17 were rejected under 35 U.S.C. § 102(b) as being anticipated by Lake *et al.* U.S. 6,087,731 ("Lake"). As to claims 1, 12 and 15, the Examiner asserts:

> Lake teaches a method of encapsulating flip chip interconnects comprising application of a limited quantity of resin 32 (see figure 4) to the interconnect bumps 24 of a IC chip 20,22. The step of applying resin, as taught by Lake, comprises dipping the IC chip with interconnect bumps 24 into a pool of the resin 32 and then withdrawing the IC chip from the pool of resin 32. Thereafter, the IC chip device can be bonded to other substrates.

This rejection is traversed. Lake does not teach or suggest encapsulation. The resin 32 in Lake is a **conductive resin** and, together with the bumps 24, forms a conductive bump structure.

Lake describes increasing the height of conductive flip chip bump structures, by forming a bump of conductive material over a substrate and dipping at least a portion of the bump into a

volume of a conductive flowable material, with some of the flowable material remaining over the bump. The remaining flowable material over the bump is solidified. The solidified flowable material together with the conductive material of the bump provide a bump assembly having a height greater than that of the original bump. Referring to Lake FIG. 3 (and the Lake specification referring thereto), electrically conductive bumps 24 are formed over the substrate 20 (or individual die 22), making contact with bond pads (not shown in the FIGS.), which enable connections to be made between the chip and circuitry or components which are external to the chip. Referring to Lake FIGS. 4 and 5, a volume of **conductive** flowable material 32 is provided over a surface 43 to a desired thickness. The conductive flowable material 32 may be a conductive epoxy, for example. Referring to Lake FIGS. 6 - 8, the bumps 24 are immersed into and then removed from the conductive flowable material 32, so that at least some of the flowable material 36 remains over the bumps 24, and then the bumps are exposed to conditions effective to at least partially solidify the flowable material 36. In Lake FIG. 9, the solidified material 36 together with the original bump 24 provides a bump assembly 38 having a greater height than the original bump. In some embodiments, as shown in FIG. 10, a further increase in bump height may be provided by an additional step of dipping in a conductive flowable material 32. In FIGS. 11 - 14, conductive bumps 24a are immersed into and then removed from a conductive flowable material 32, and the remaining conductive material 36a is engaged with a planar surface to flatten the remaining conductive material 36a and thereby to provide a flip chip bump assembly 38a having a generally planar uppermost surface 48 away from the substrate.

Lake has nothing to do with encapsulation; insulation, encapsulation, molding, are not even mentioned. Lake is directed to conductive bump structures; Lake describes bump structures, in which flowable **conductive** materials are used to increase the height of bump structures. The flowable materials in Lake must necessarily be conductive, as they are part of the electrical interconnect between the die and the substrate.

Applicants claims all recite the step of "applying a limited quantity of encapsulating resin" to ... an interconnect side of an integrated circuit chip. That is not suggested in Lake, and even less is it taught and, accordingly, the rejections over Lake should be withdrawn.

In view of the foregoing, all the claims now in the application are believed to be in condition for allowance, and action to that effect is respectfully requested.

This Amendment is being filed within the second month following the shortened statutory period set by the Examiner and, accordingly, it is accompanied by a petition and a fee or fee authorization for two months' extension of time. If the Examiner determines that a further extension of time is required in connection with the filing of this paper, petition is hereby made therefor, and the Commissioner is authorized to charge the fee to Deposit Account 50-0869 (Order No. CPAC 1011-2).

If the Examiner determines that a conference would further prosecution of this application, the Examiner is invited to telephone Applicants' representative, undersigned, at the telephone number set out below.

Respectfully submitted,

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